IN THE CLAIMS:

Please amend claims 1, 5-9, 15, 16, 19, 24-27, 33 and 34. Claims 2-4, 10-14, 20-23, and 28-32 have been cancelled. Claims 17, 18, 35 and 35 remain unchanged. New claims 37 and 38 have been added. All claims are listed for the convenience of the Examiner.

1. (Currently Amended) A method, comprising:

executing an instruction that updates data in a register at a first time;

storing an instruction address of the instruction;

[marking the instruction as a slowable instruction] when the data is not read from the register at a next clock cycle from completion of execution of the instruction, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address of the instruction is encountered a second time and the bit indicates that the instruction is a slowable instruction, delaying processing of the instruction.

2 – 4. (Cancelled)

5. (Currently Amended) The method of claim [4] 1, wherein when the instruction address of the instruction is encountered the second time, the [stored entry] bit is [used] examined to determine if the instruction is a slowable instruction.

6. (Currently Amended) The method of claim [4] 1, wherein delaying the processing of the instruction comprises delaying decoding the instruction.

7. (Currently Amended) The method of claim [4] 1, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

8. (Currently Amended) The method of claim [4] 1, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

9. (Currently Amended) A method, comprising:

recording a first clock cycle when an instruction that loads data into a register is to complete;

storing an instruction address of the instruction;

recording a second clock cycle when the data is read from the register; [and]

[making the instruction as a slowable instruction] when the second clock cycle is more than [a predetermined time threshold] one clock cycle from the first clock cycle, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address is encountered a next time, and the bit indicates that the instruction is the slowable instruction, delaying processing of the instruction.

10 – 14. (Cancelled)

15. (Currently Amended) The method of claim [14] 9, wherein the processing of the instruction is delayed by delaying decoding the instruction.

16. (Currently Amended) The method of claim [14] 9, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

17. (Original) The method of claim 9, wherein information about the first clock cycle and the second clock cycle is provided by a scheduler.

18. (Original) The method of claim 17, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.

19. (Currently amended) A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:
executing an instruction that loads data into a register at a first time; and
storing an instruction address of the instruction;
[marking the instruction as a slowable instruction] when the data is not read from the register at a next clock cycle from completion of execution of the instruction, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and
when the instruction address of the instruction is encountered a second time and the bit indicates that the instruction is a slowable instruction, delaying processing of the instruction.

20 - 23. (Cancelled)

24. (Currently Amended) The computer readable medium of claim [22] 19, bwherein delaying the processing of the instruction comprises delaying decoding the instruction.

25. (Currently Amended) The computer readable medium of claim [22] 19, wherein delaying the processing of the instruction comprises using lower priority resources to execute the instruction.

26. (Currently Amended) The computer readable medium of claim [22] 19, wherein delaying the processing of the instruction comprises delaying loading the data into the register until prior to the data is read from the register.

27. (Currently Amended) A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

recording a first clock cycle when an instruction is to complete [loading] storing data in a register;

storing an instruction address of the instruction;

recording a second clock cycle when the data is read from the register; [and]

[making the instruction as a slowable instruction] when the second clock cycle is more than [a predetermined time threshold] one clock cycle from the first clock cycle, setting a bit associated with the instruction address to indicate that the instruction is a slowable instruction; and

when the instruction address is encountered a next time, and the bit indicates that the instruction is the slowable instruction, delaying processing of the

instruction.

28 - 32. (Cancelled)

33. (Currently Amended) The computer readable medium of claim [32] 27, wherein the processing of the instruction is delayed by delaying decoding the instruction.

34. (Currently Amended) The computer readable medium of claim [32] 27, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.

35. (Original) The computer readable medium of claim 27, wherein information about the first clock cycle and the second clock cycle are provided by a scheduler.

36. (Original) The computer readable medium of claim 35, wherein the scheduler provides the information about the first clock cycle and the second clock cycle prior to execution of the instruction.

37. (New) A system, comprising:

a processor; and

an instruction to be executed by the processor, wherein processing of the instruction is to delay at a second time when a result of the instruction stored in a register at a first time is not immediately used by one or more

subsequent instructions, wherein the instruction is marked as can be delayed after the first time and before the second time.

38. (New) The system of claim 37, wherein the processing of the instruction is delayed by using lower priority resources to execute the instruction.